IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor device, comprising:

a multilayer wiring structure including a plurality of wiring layers formed on a substrate;

a capacitor arranged in a predetermined wiring layer in the multilayer wiring structure and including a lower electrode, a dielectric film, and an upper electrode;

a first via formed in the predetermined wiring layer and connected directly to a top surface of the upper electrode of the capacitor; and

a second via formed in an overlying wiring layer stacked on the predetermined wiring layer, the second via being connected directly on the first via and the second via being connected to a wiring formed in the overlying wiring layer,

wherein the first via is formed to have a larger cross section than that of the second via.

Claim 2 (Canceled).

Claim 3 (Original): A semiconductor device according to claim 1, wherein the predetermined wiring layer has a third via formed on the lower electrode and a wiring connected to the third via and buried in a surface of the predetermined wiring layer.

Claim 4 (Currently Amended): A semiconductor device according to claim [[2]] 1, wherein the predetermined wiring layer has a third via formed on the lower electrode and a wiring connected to the third via and buried in a surface of the predetermined wiring layer.

Claim 5 (Previously Presented): A semiconductor device according to claim 3, wherein the wiring comprises copper, and a copper diffusion stopper film is formed on the surface of the predetermined wiring layer to prevent diffusion of the copper forming the wiring.

Claim 6 (Previously Presented): A semiconductor device according to claim 4, wherein the wiring comprises copper, and a copper diffusion stopper film is formed on a surface of the predetermined wiring layer to prevent diffusion of the copper forming the wiring.

Claim 7 (Original): A semiconductor device according to claim l, wherein the overlying wiring layer has a wiring connected to a top of the second via and buried in a surface of the overlying wiring layer.

Claim 8 (Currently Amended): A semiconductor device according to claim [[2]] 1, wherein the overlying wiring layer has a wiring connected to a top of the second via and buried in a surface of the overlying wiring layer.

Claim 9 (Currently Amended): A semiconductor device ~~according to claim 1~~ comprising:

a multilayer wiring structure including a plurality of wiring layers formed on a substrate;

a capacitor arranged in a predetermined wiring layer in the multilayer wiring structure and including a lower electrode, a dielectric film, and an upper electrode;

a first via formed in the predetermined wiring layer and connected directly to a top surface of the upper electrode of the capacitor; and

a second via formed in an overlying wiring layer stacked on the predetermined wiring layer, the second via being connected directly on the first via and the second via being connected to a wiring formed in the overlying wiring layer,

wherein a third via formed on the lower electrode of the capacitor is provided in the predetermined wiring layer; a fourth via formed connected to a top of the third via and formed to be thinner than the third via is provided in the overlying wired layer; and

the second and fourth vias are connected to the first and second wirings, respectively, buried in a surface of the overlying wiring layer.

Claim 10 (Currently Amended): A semiconductor device according to claim [[2]] 1, wherein a third via formed above the lower electrode of the capacitor is provided in the predetermined wiring layer;

a fourth via connected on the third via and formed to be thinner than the third via is provided in the overlying wiring layer; and

the second and fourth vias are connected to the first and second wirings, respectively, buried in a surface of the overlying wiring layer.

Claim 11 (Original): A semiconductor device according to claim 1, wherein the lower electrode of the capacitor is connected to a wiring buried in a surface of an underlying wiring layer formed under the predetermined wiring layer in which the capacitor is formed.

Claim 12 (Currently Amended): A semiconductor device according to claim [[2]] 1, wherein the lower electrode of the capacitor is connected to a wiring buried in a surface of an

underlying wiring layer formed under the predetermined wiring layer in which the capacitor is formed.

Claim 13 (Previously Presented): A semiconductor device, comprising:

at least one impurity diffusion layer formed in a first area of a semiconductor substrate;

a plurality of wiring layers stacked on the semiconductor substrate and including a first wiring layer having a contact connected to the impurity diffusion layer and a first wiring buried in the first wiring layer and connected to the contact;

a capacitor formed in a predetermined one of the plurality of wiring layers which predetermined wiring layer is formed on a second area different from the first area of the semiconductor substrate, the capacitor having a stacked structure of a lower electrode, a dielectric film, and an upper electrode;

a first via connected directly on at least the upper electrode formed in the predetermined wiring layer;

an upper wiring layer having an interlayer insulating film stacked on the predetermined wiring layer, a second via formed in the interlayer insulating film, connected directly to the first via, and formed to be thinner than the first via, and a second wiring connected directly to the second via and buried in a surface portion of the upper wiring layer.